(6b) TE (SEM: VI) (Rev: 2012) (CBSGS) ETRX 10/5/16

Basic VLSI Design

Q.P. Code : 591600

(3 Hours) **[Total Marks :80**

N.B. : (1) **Question** No.**1** is compulsory.
(2) Attempt any **three** out of remaining.
(3) Assume suitable data wherever required.

1. (a) Draw and explain AND gate using pass transistor logic. **20**
(b) Explain drawhack of dynamic CMOS design.
(c) Draw and explain manchester carry circuit.
(d) What are various programming techniques used for EEPROM in Explain them in short.

2. (a) Draw 6T SRAM cell and explain it's read and write operation. **10**
(b) Define scaling ? Explain various types of scaling in detail. **10**

3. (a) Explain latch up condition in CMOS in detail. What are remedies to avoid latchup. **10**
(b) Give and explain the drawback of ripple carry adder. Explain 4 bit CLA adder with it's carry equations, logical network using dynamic CMOS logic. **10**

4. (a) Explain how ESD (electrostatic discharge) affect the MOSFET. Give and explain input protection circuits. **10**
(b) Give and explain interconnect scaling with its width, length, thickness and capacitances. **10**

5. (a) Explain various technique of clock generation. Discuss 'H' tree clock distribution. **10**
(b) Consider a CMOS inverter circuits with following parameters **10**

VDD = 3.3v VTon = 0.6v VTop = - 0.7v, $\mu_n C_{ox}$ = 60 μ A/v², $\left(\frac{W}{L}\right)_n$ = 8

$\mu_p C_{ox}$ = 20 μA/V², $\left(\frac{W}{L}\right)_p$ = 12. Calculate the noise margin.

6. Write a short note on **20**
(1) Sense ampliter
(2) Barrel shifter
(3) Interconnect parameters

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TE- SEM :V) (R-2012) (CBSGS)-ETRX 7/6/2016

MITM

Q. P. Code : 592100

(2 Hours) **Total Marks-40**

Note:

i. Q.1 is compulsory
ii. Attempt any three questions from remaining five.
iii. Each question carries **10** marks.

1. Answer any five.

a. Write any four top security concerns. **2**
b. Define OSI layers. **2**
c. Write a small note on E-business. **2**
d. What is search engine? **2**
e. Explain network management. **2**
f. What is data mining? **2**
g. Which are the components of IT Infra? **2**

2.

a. Define topology. Explain any three common topologies. **5**
b. Define cabling. Classify cable types and explain in detail. **5**

3.

a. Explain open source software with examples. **5**
b. Write a detailed note on firewall. **5**

4.

a. Explain the benefits of intranet. **5**
b. State the types of network. How is optical network different from wired network? **5**

5.

a. Discuss the TCP/IP stack. Also list the various functions of the internet protocol.5
b. Explain the following terms related to storage. **5**
i) Online storage
ii) Near line storage
iii) Offline storage

6. Write a note on following terms related to IT audit. **10**
i) Information audit.
ii) Audit schedule
iii) Audit plan
iv) Audit preparation
v) Internal audit.

TE (Electronics) Sem VI (CBGS)

Advance Instrumentation Systems

QP Code : 591702

16-05-2018

(3 Hours) **[Total Marks : 80**

N.B. (1) Question No.1 is **compulsory.**
(2) Attempt any three questions from remaining five quesitons.
(3) Assume suitable data if necessary.
(4) Figures to the right indicate full marks.

1. (a) With neat block diagram, explain the working of multichannel data acquisition system. **10**
   (b) Why converters are required? Explain electrical to pneumatic converter. **10**

2. (a) Draw and explain single and double acting actuators. **10**
   (b) Explain the installation procedure of control valve. **10**

3. (a) Explain the working of smart transmitters. Highlight the features of smart transmitter. **10**
   (b) With neat diagram, explain the cascade of PID controller. **10**

4. (a) Compare electrical, pneumatic and hydraulic actuators. **10**
   (b) Draw and explain inherent and installed characteristics of control valves. **10**

5. (a) With neat diagram, explain the instrument air system. **10**
   (b) Explain the working of electronic DP transmitter. **10**

6. (a) Explain process reaction curve method and ZN method of PID tuning. **10**
   (b) With neat diagram, explain speed control circuit for hydraulic actuator. **10**

T. E. SEM VI CBGS
1/06/16
ETRX
Digital Signal processing and processors

Q.P. Code : 592000

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **three** questions from remaining questions.
(3) Assume suitable **data** wherever **necessary**.

1. (a) Explain Quantization and effects of truncation and rounding. **20**
(b) Compare Butterworth and Chebyshev filters.
(c) What is DTFS. Find DTFS of
$x(n) = \{0,1,2,3\}$ with period, $N = 4$.
(d) Explain the concept of Pipelining in Digital Signal Processors.

2. (a) If $X(n) = n+1$ and $N = 8$, Find $X(k)$ using DIF-FFT algorithm. **10**
(b) Given $X(k) = \{20, -5.828 - j2.414, 0, -0.172 - j\,0.414, 0, -0.172 + j\,0.414, 0, -5.828 + j2.414\}$ Find the sequence $x(n)$ using Inverse FFT algorithm. **10**

3. (a) Design a Butterworth digital IIR Lowpass filter using Impulse Invariant transformation method for the following specifications. **10**

$0.707 \le |H(e^{iw})| \le 1.0$ for $0 \le w \le 0.3\pi$

$|H(e^{iw})| \le 0.2$ for $0.75\pi \le w \le \pi$

(T = 1sec)

(b) Write down design steps for FIR filter using window techniques. Compare windows. **10**

4. (a) A discrete time system has a tansfer function **10**

$$H(z) = \frac{1}{1 - 0.8z^{-1} + 0.12z^{-2}}$$

A four bit processor is used in which MSB represents sign bit and remaining 3 bits store quantized co-efficients.

(i) What is the effect of quantization on pole location if direct form II is used for relization.
(ii) If cascade form is used for relization, then what is the change in the pole values after quantization.
(iii) In which case (direct form II or Cascade) the shift from the actual pole location due to quantization is less?

(b) Explain the following terms. **10**
(i) Zero input limit cycle
(ii) Dead band
(iii) Truncation
(iv) Rounding

[TURN OVER

5. (a) Explain Von-Neumann Architecture, Harvard Architecture and modified Harvard architecture in details. How architecture of advanced Digital signal processor is different from modified Harvard architecture. **10**

(b) Explain VLIW Architecture in detail. **10**

6. Write short notes on **20**
   (a) Gibb's phenomenon
   (b) Applications of Digital Signal Processors in Biomedical and Audio
   (c) Frequency Transformation in IIR filters.

Sem-VI (CBGS) ETRX 20/5/16.

Computer Organization

Q.P. Code : 591801

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **No.1** is **compulsory**.
(2) Attempt **any Three** questions from remaining **questions**.
(3) **All** questions carry **equal marks**.
(4) **Figures** to the **right** indicate **full marks**.

1. (a) Explain single and double precision format for floating point number representation. **5**
(b) Write in brief on nano-programming. **5**
(c) Draw Register structure of IA-32 family. **5**
(d) Explain SIMD computer organization. **5**

2. (a) Explain performance measure of computer architecture and factors to improve the performance of the system. **10**
(b) What is microprogramming ? Draw and explain Micro programmed control unit. **10**

3. (a) Explain sequence counter method of implementing Hardware control unit. **10**
(b) What is LRU Algorithm? Find the page fault for the following string using FIFO and LRU page replacement policies for the page address stream 6 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 5. Consider page frame size n = 3. **10**

4. (a) What are the different cache mapping techniques? **10**
Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048 (2k) words and assume that the main memory is addressable by a 16 bit address and it consists of 4k blocks. How many bits are there in each of the TAG, BLOCK/SET and WORD fields for different mapping techniques.
(b) Explain in brief about various DMA transfer modes. **10**

5. (a) Explain Address translation with respect to virtual memory. Hence explain use of Translation Look aside Buffer (TLB). **10**
(b) Compare RISC and CISC architectures. **5**
(c) Write a note on addressing modes of IA- 32 family. **5**

6. (a) Explain data hazard and code hazard in pipelining. Mention solutions to minimize the hazards. **10**
(b) What is bus contention? How is it resolved by using bus arbitration? Explain various bus arbitration methods. **10**

SEM VI E7RX CBSGS RC

POWER ELECTRONICS-I

D+ 26/05/2016

QP Code :591902

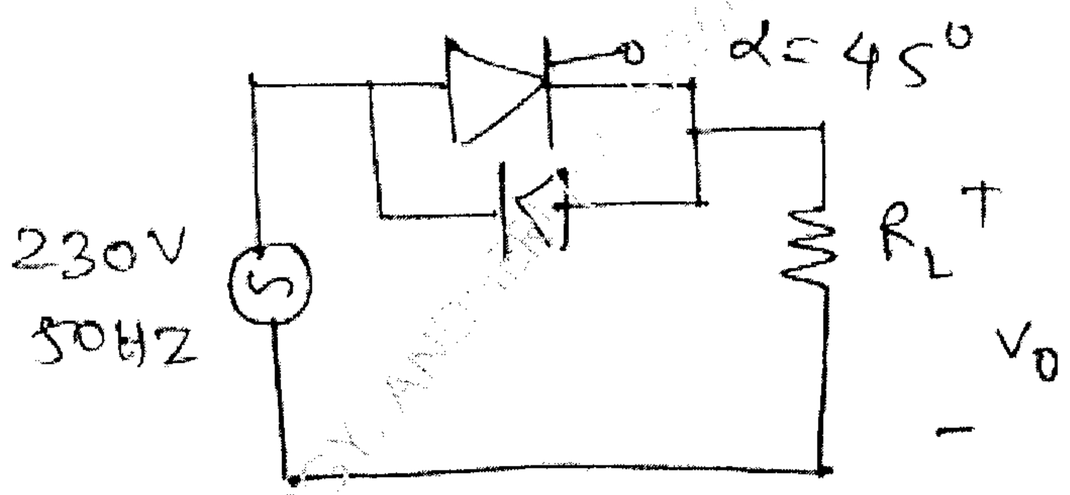
(3 Hours) **| Total Marks :80**

N.B. : (1) **Question** No. **1** is **compulsory**.
(2) Attempt any **three** questions out of remaining **five** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Draw and explain dynamic turn on characteristics of SCR **5**
(b) What is the need of commutation. Explain the any one method of forced communication. **5**
(c) Define and explain performance parameters of controlled rectifier **5**
(d) Draw and explain boost converter. Derive the relation for output load voltage. **5**

2. (a) Draw and explain semi-converter with the help of circuit diagram and waveforms. **10**
(b) Draw and explain Buck-Boost converter with the help of circuit diagram and waveforms Derive the relation for load voltage. **10**

3. (a) Explain the working of three phase bridge inverter in 120^0 conduction mode with resistive load. Draw waveforms. **5**
(b) Draw the load voltage waveform for the circuit given below. **5**



(c) draw and explain SOA of power MOSFET. **5**

4. (a) A single phase semi converter is operated from 230V, 50Hz ac supply. The load resistance is 20Ω. The average output voltage is 30% of the max. Possible average output voltage. Determine **10**
(i) Firing angle
(ii) RMS and Average output current
(iii) RMS and average thyristor current
(b) Explain in brief single phase cyclo-converter with circuit diagram and waveforms. **5**

[Turn Over

(c) Explain the need of neutrilisation of harmonics of inverters. **5**

5. (a) Explain the working of AC full wave control circuit using DIAC-TRIAC. **10**
Draw waveforms across load and TRFAC for $\alpha = 60^0$. Derive relation for RMS load voltage.

(b) Explain the multiple pulse width modulation in inverters. Explain the neutrilisation of harmonics. **10**

6. (a) Single phase full bridge inverter has a resisistive load of R = 3Ω and the dc input voltage Edc = 50V. compute **10**
   (i) The average output power Po
   (ii) The average and peak current of each thyristor.

(b) Draw and explain switching cha. of GTO **5**

(c) Draw and explain snubber circuit. **5**
